

40V N-Channel Power SpeedFET

• General Description

It combines trench MOSFET technology with a low resistance package to provide extremely low  $R_{DS(ON)}$ .

• Features

- AEC-Q101 Qualified
- Low  $R_{DS(ON)}$  to minimize conductive loss
- High GOX reliability
- Low Thermal resistance

• Application

- BLDC Motor driver
- DC-DC
- Battery protection

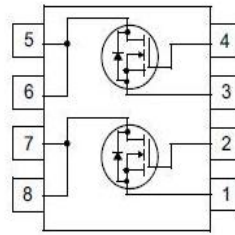
• Ordering Information:

Part NO.	ZMDA68406N
Marking	ZMD68406
Packing Information	REEL TAPE
Basic ordering unit (pcs)	3000

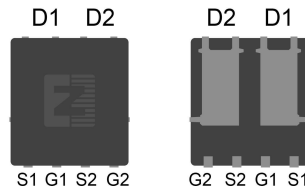
• Absolute Maximum Ratings ( $T_C=25^\circ\text{C}$ )

Parameter	Symbol	Conditions	Value	Unit
Drain-Source Voltage	$V_{DS}$		40	V
Gate-Source Voltage <sup>①</sup>	$V_{GS}$		$\pm 20$	V
Continuous Drain Current	$I_D$	$T_C=25^\circ\text{C}$	45	A
	$I_D$	$T_C=75^\circ\text{C}$	38	A
	$I_D$	$T_C=100^\circ\text{C}$	33	A
Pulsed Drain Current	$I_{DM}$	Pulsed; $t_p \leq 10 \mu\text{s}$ ; $T_{mb} = 25^\circ\text{C}$ ;	180	A
Total Power Dissipation	$P_D$	$T_C=25^\circ\text{C}$	42	W
Total Power Dissipation	$P_D$	$T_A=25^\circ\text{C}$	3.3	W
Operating Junction Temperature	$T_J$		-55 to +175	$^\circ\text{C}$
Storage Temperature	$T_{STG}$		-55 to +175	$^\circ\text{C}$
Single Pulse Avalanche Energy	$E_{AS}$	$L=0.1\text{mH}$ , $V_{GS}=10\text{V}$ , $R_g=25\Omega$ ,	40	mJ
		$L=0.5\text{mH}$ , $V_{GS}=10\text{V}$ , $R_g=25\Omega$ ,	84	mJ
ESD Level (HBM)	CLASS 1C			

• Product Summary



$V_{DS} = 40\text{V}$   
 $R_{DS(ON)} = 6.2\text{m}\Omega$   
 $I_D = 45\text{A}$



DFN5\*6



**•Thermal resistance**

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	$R_{thJC}$		-	3.6	$^{\circ}C/W$
Thermal resistance, junction-ambient <sup>②</sup>	$R_{thJA}$		-	45	$^{\circ}C/W$
Soldering temperature	$T_{sold}$		-	260	$^{\circ}C$

**•Electronic Characteristics**

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	40			V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2	2.7	4	V
Drain-Source Leakage Current	$I_{DSS}$	$V_{GS} = 0V, V_{DS} = 40V$			1.0	$\mu A$
Gate- Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20V, V_{DS} = 0V$			100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 14A$		6.2	7.5	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS} = 5V, I_{SD} = 10A$		7		S
Diode Forward Voltage	$V_{FSD}$	$V_{GS} = 0V, I_{SD} = 14A$			1.3	V

**•Dynamic characteristics**

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	$C_{iss}$	$f = 1MHz, V_{DS} = 25V$	-	845	-	pF
Output capacitance	$C_{oss}$		-	236	-	
Reverse transfer capacitance	$C_{rss}$		-	18	-	
Gate Resistance	$R_g$	$f = 1MHz$	-	1.6		$\Omega$
Total gate charge	$Q_g$	$V_{DD} = 15V, I_D = 20A, V_{GS} = 10V$	-	17	-	nC
	$Q_g (4.5v)$		-	9	-	
Gate - Source charge	$Q_{gs}$		-	2.7	-	
Gate - Drain charge	$Q_{gd}$		-	5.3	-	
Turn-ON Delay time	$t_{D(on)}$		$V_{GS} = 10V, V_{DS} = 15V, R_G = 3.3\Omega, I_D = 20A$	-	5	
Turn-ON Rise time	$t_r$	-		10	-	ns
Turn-Off Delay time	$t_{D(off)}$	-		8	-	ns
Turn-Off Fall time	$t_f$	-		3	-	ns
Reverse Recovery Time	$t_{RR}$	$V_{DD} = 20V, di_s/dt = 100A/\mu s, I_S = 20A$	-	8	-	ns
Reverse Recovery Charge	$Q_{RR}$		-	17	-	nC

Fig.1 Gate-Charge Characteristics

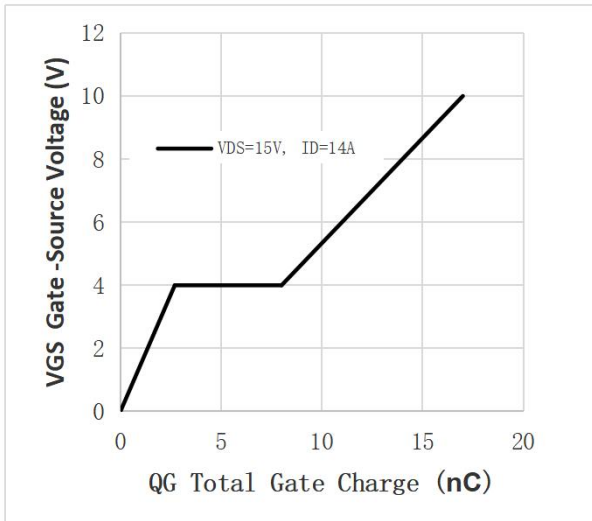


Fig.2 Capacitance Characteristics

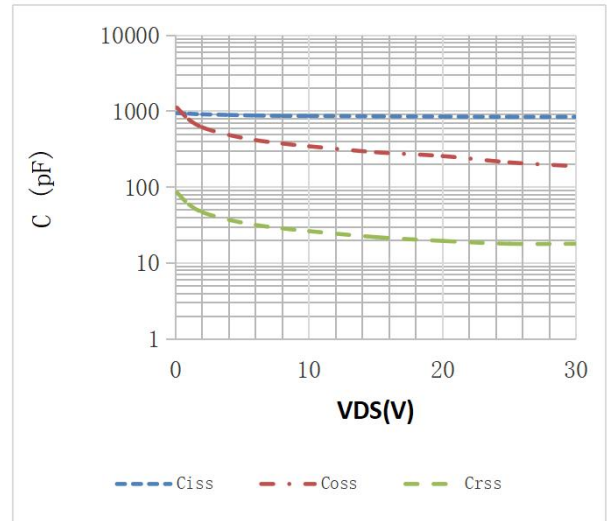


Fig.3 Power Dissipation

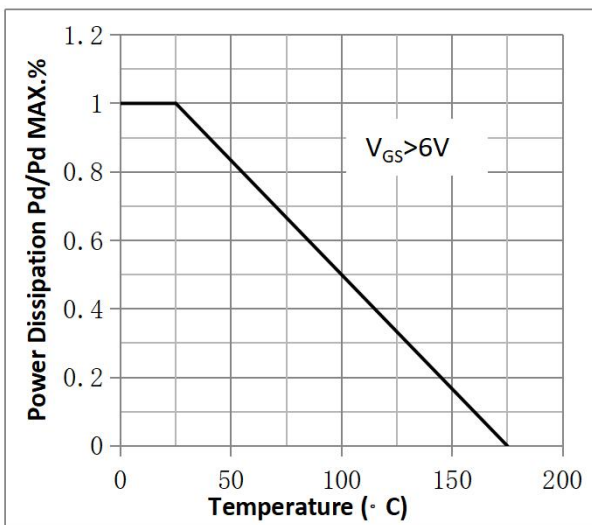


Fig.4 Typical output Characteristics

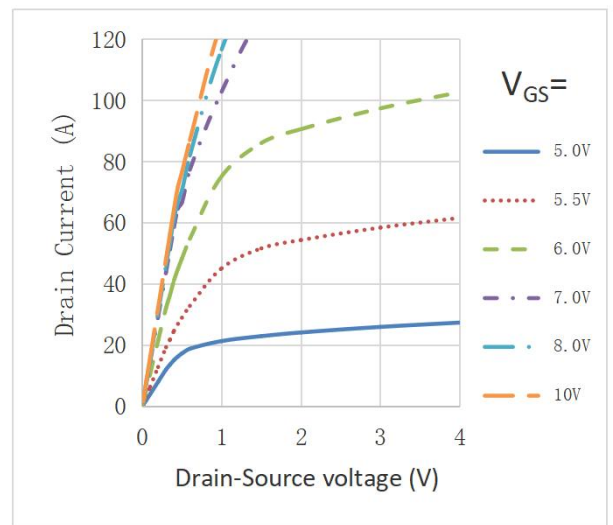


Fig.5 Threshold Voltage V.S Junction Temperature

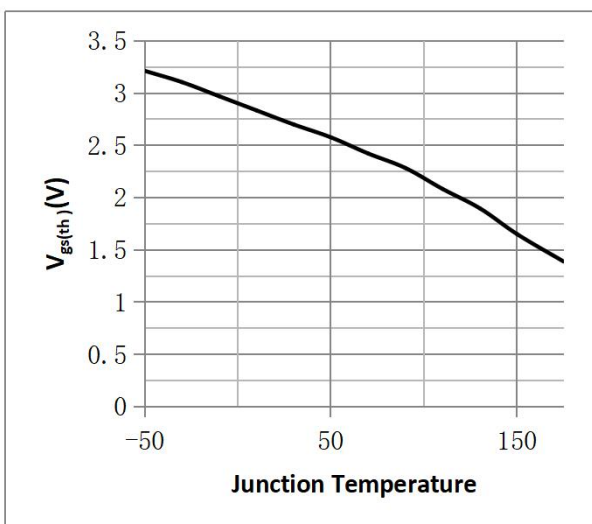


Fig.6 Resistance V.S Drain Current

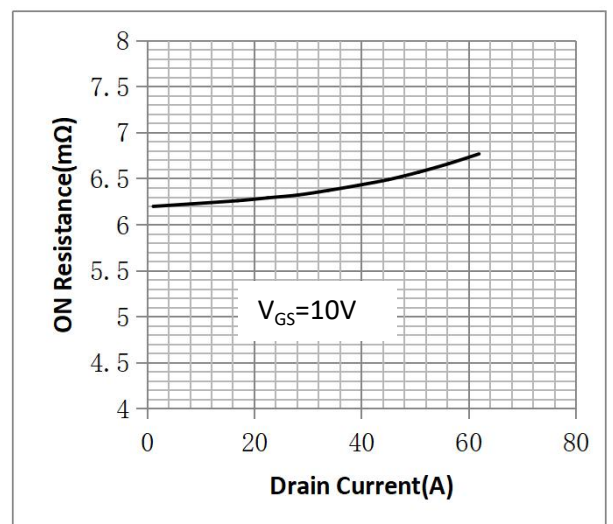


Fig.7 On-Resistance VS Gate Source Voltage

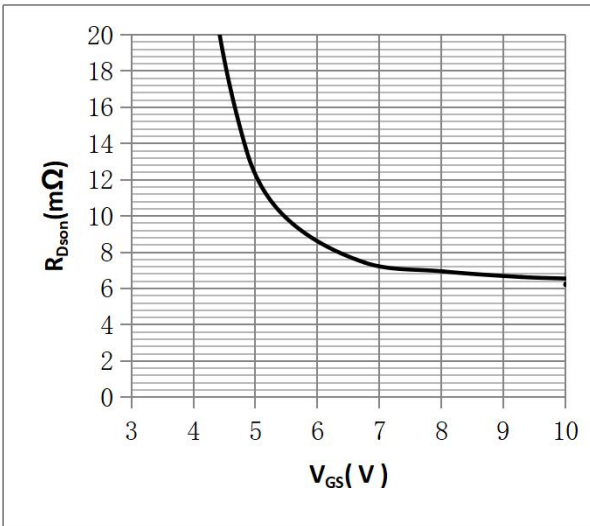


Fig.8 On-Resistance V.S Junction Temperature

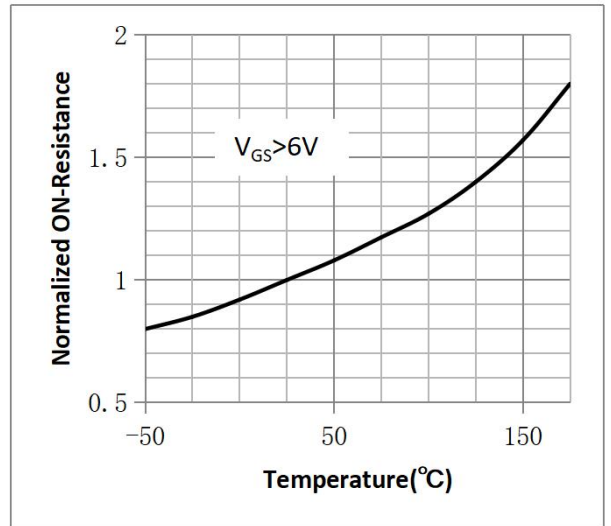


Figure 9. Diode Forward Voltage vs. Current

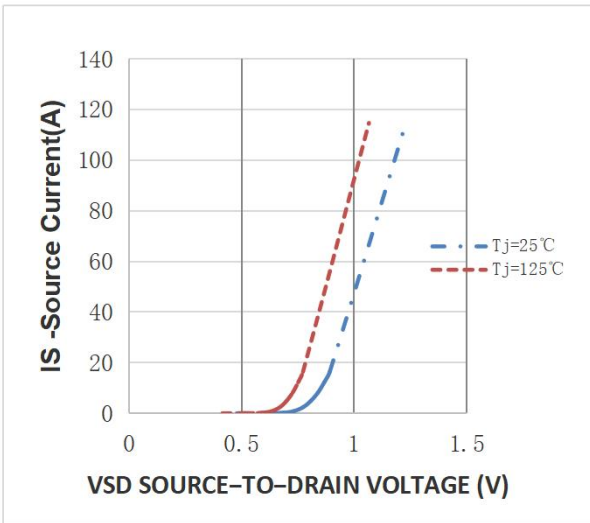


Figure 10. Transfer Characteristics

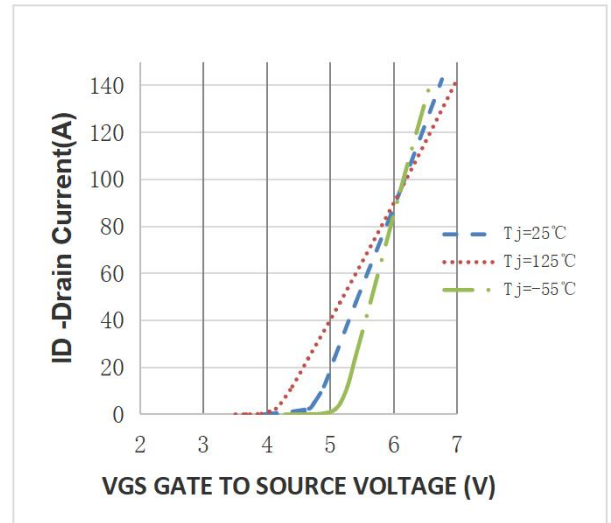


Fig.11 Safe Operating Area

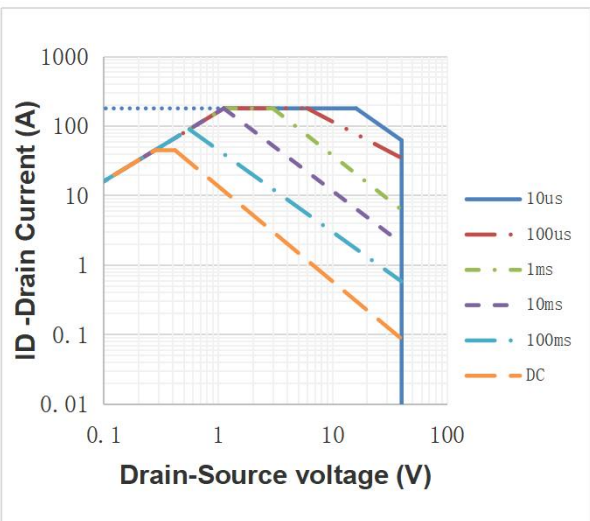
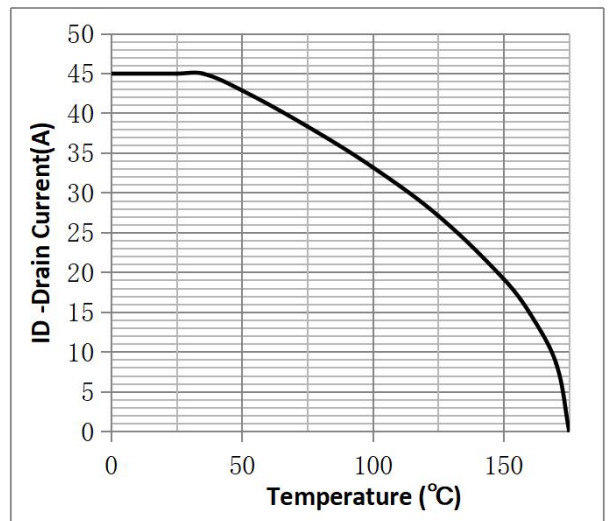
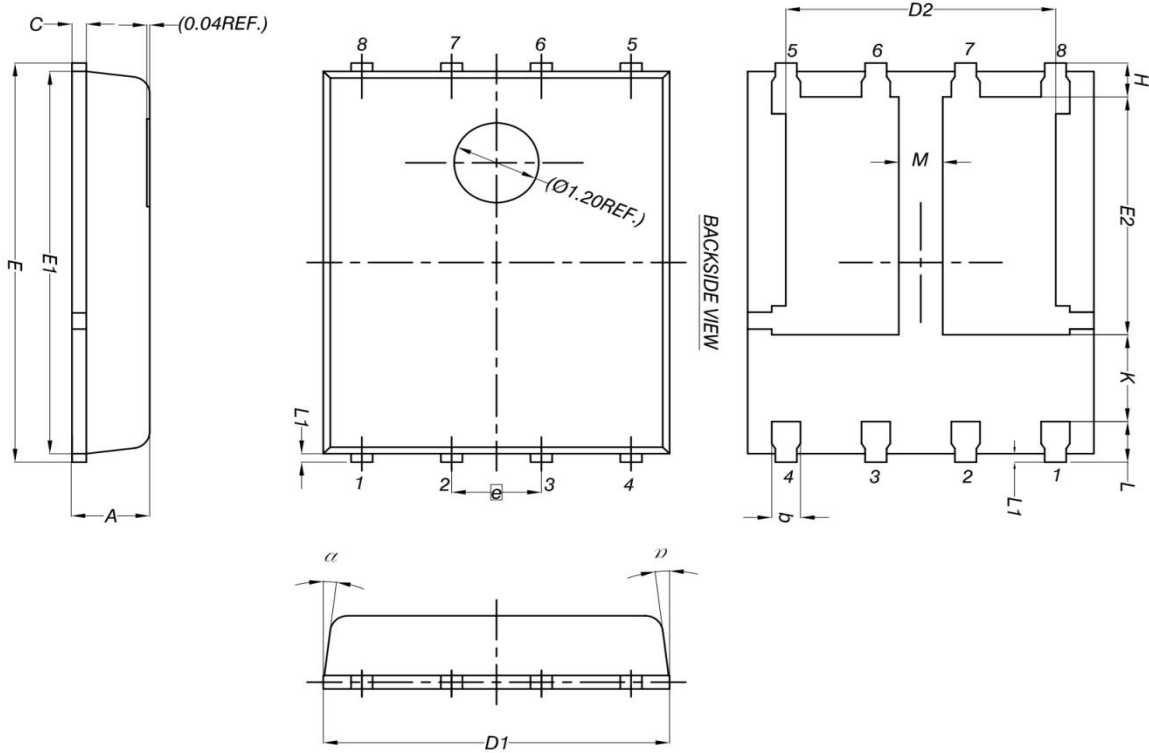


Fig.12 ID vs. Junction Temperature<sup>③</sup>

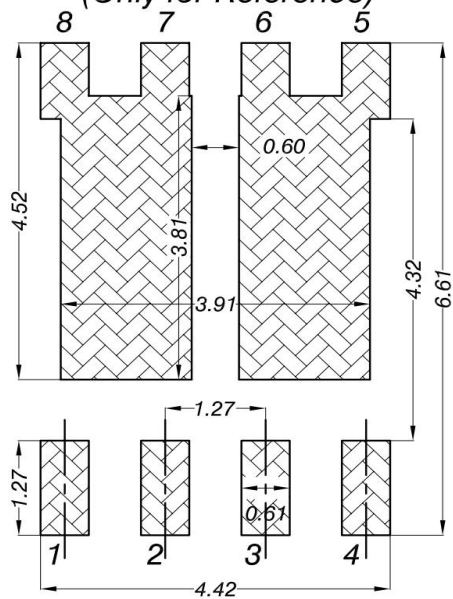


•DFN5\*6 Package Outline



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
$e$	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
M	0.50	-	-
$\alpha$	0°	-	12°

Land Pattern  
(Only for Reference)



**Note:**

- ① Pulse :  $V_{GS}=+20V/-20V$ , Duty cycle=50%,  $T_j=175^{\circ}C$ ,  $t=1000$  hours; For DC , the following test conditions can be passed:  $V_{GS}=+20V/-10V$ ,  $T_j=175^{\circ}C$ ,  $t=1000$  hours;
- ② Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate;
- ③ Practically the current will be limited by PCB, thermal design and operating temperature.  $V_{GS}=10V$ .

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## Revision History

Version	Date	Change
A	2021.11.3	
B	2022.9.5	1.Add Reach,HF figure
C	2022.10.10	The upper limit of Rdson is tightened to 8.1mΩ
D	2023.3.10	Modified Rdson upp limit TO 7.5mΩ
E	2023.3.30	Correct QG,ouline dimension,